AMENDMENTS TO THE SPECIFICATION:

Page 1, before line 3, insert the following headings:

--BACKGROUND OF THE INVENTION

Field of the Invention--

Page 1, between lines 8 and 9, insert the following heading:

--DESCRIPTION OF THE RELATED ART--

Page 2, between lines 2 and 3, insert the following heading:

--BRIEF SUMMARY OF THE INVENTION--

Page 10, between lines 9 and 10, insert the following heading:

--BRIEF DESCRIPTION OF THE DRAWING FIGURES--

Page 11, between lines 5 and 6, insert the following heading:

--DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS--

Page 15, replace the paragraph beginning on line 6 with the following amended paragraph:

--In the case of Figure 8, the components are self tested independently. The results are fed to a summator 6 and latched until the next test result for a component is received. The test may be for an individual component that has been tested a set number of times or over a set time period to achieve a single set of results for that component with the results being summated. Alternatively, results for different components can be

fed to the summator 6 and latched until a set number of test results for separate components is achieved. The latched results are then sent to a processor [[3]] 7, which conducts a self test upon response from an input from the summator 6. The processor 7 can operate as a result of a response from a single signal from a test button or upon receiving a signal from the base charger from a server controlling the test apparatus. In this case, the operator of the self test can check the self test status using the indicator 4 or alternatively the processor 7 looks at the summator self status. This arrangement allows the indicator to be operated independently of the processor and directly from the summator 6.--

Page 15, replace the paragraph beginning on line 21 and bridging pages 15 and 16 with the following amended paragraph:

--As shown in Figure 9, the indicator 4 may be directly linked to the self test facility 5 for the components [[5]]. The self test facility 5 can be provided ~~as a~~ in the form of a test processor 7 that produces for example a signal. A typical test processor will be a 555 timer having a clock counter, which will provide about 60 pulses per minute to, for example pads. A current drop through the pads equals impedance and the test processor in the pad can measure the impedance. A signal is [[then]] generated which is then fed to the summator 6 and latched until the next result from a measurement of the impedance is passed to the summator 6. [[The]] A processor 7 then

calculates the values of a series of results from the summator 6 or a combined result from the summator 6 to see if it falls within certain values for the component and the whole result can then be indicated to display whether the component is in a condition to operate.--

Page 16, replace the paragraph beginning on line 6 with the following amended paragraph:

--Figure 10 shows a particular embodiment where separate input lines for in this case five components are fed to the summator 6 and two output lines are fed through the summator 6, one to the processor [[6]] 7 and one to the indicator 4 [[-]]. Information from the summator 6 then passes to the to the indicator 4 for display.--